IN THE CLAIMS

1. (Original) A content addressable memory (CAM) device for comparing a search key to data values stored therein, comprising:

a plurality of CAM blocks, each CAM block including an array of CAM cells divided into a plurality of segments, each array segment for storing a number of data values that are assigned the same priority; and

a plurality of block priority circuits, each having inputs to receive match signals from a corresponding CAM block, outputs to generate a block index and the priority of a matching data value, and an address table for storing address information for each array segment in the corresponding CAM block.

2. (Original) The CAM device of Claim 1, wherein each CAM block is assigned to store a predetermined content range of data values.

3. (Original) The CAM device of Claim 1, further comprising an overflow CAM block that can store any data value, regardless of content.

4. (Original) The CAM device of Claim 1, further comprising:

means for extracting a selected portion of the search key in response to a select signal; and

means for selectively enabling each CAM block in response to a comparison between the selected portion of the search key and the predetermined range of data values for the corresponding CAM block.

5. (Original) The CAM device of Claim 1, wherein the address information comprises a start address for each array segment.

6. (Original) The CAM device of Claim 1, wherein the address information comprises an address range for each array segment.

7. (Original) The CAM device of Claim 1, wherein each block priority circuit compares the block index with the address information to determine the priority assigned to the matching data value.

8. (Original) The CAM device of Claim 1, wherein each block priority circuit further comprises:

a priority encoder having inputs to receive the match signals from the corresponding CAM block and having an output to generate a row index of the matching data value;

a compare circuit having first inputs to receive the address information, a second input to receive the row index, and a plurality of outputs; and

a priority table having a plurality of rows, each for storing the priority assigned to a corresponding array segment and having an input coupled to a corresponding output of the compare circuit, the priority table having an output to generate the priority of the matching data value.

9. (Original) The CAM device of Claim 8, wherein the compare circuit compares the row index with the address information to selectively enable one of the rows of the priority table.

10. (Original) The CAM device of Claim 9, wherein the compare circuit asserts one of a plurality of priority select signals in response to the comparison between the row index and the address information.

11. (Original) The CAM device of Claim 8, wherein each block priority circuit further comprises:

a memory to store a block identification (ID) for the corresponding CAM block; and

means for concatenating the block ID to the row index to generate the block index.

12. (Original) The CAM device of Claim 1, further comprising:

a global priority and index circuit having inputs to receive the block indexes and priorities from the block priority circuits, and having an output to generate a device index of the highest priority matching data value.

13. (Original) The CAM device of Claim 12, wherein the global priority and index circuit comprises:

compare logic having inputs to receive the priorities from the block priority circuits and having outputs to generate select signals for corresponding CAM blocks; and

a select circuit having first inputs to receive the block indexes, second inputs to receive the select signals, and an output to generate the device index.

14. (Original) The CAM device of Claim 13, wherein the select circuit selectively outputs one of the block indexes as the device index in response to the select signals.

15. (Original) The CAM device of Claim 13, wherein the compare logic compares the priorities with each other to determine which priority is the highest.

16. (Original) The CAM device of Claim 15, wherein the compare logic includes a second output to generate the highest priority.

17. (Original) The CAM device of Claim 1, wherein each block priority circuit comprises:

a priority encoder and match flag circuit having a plurality of segments, each segment including inputs to receive the match signals from a corresponding array segment and having outputs to generate a row index and a segment match flag for the corresponding array segment; and

a priority circuit having inputs to receive the row indexes and segment match flags and having outputs to generate a device index and priority of a highest priority matching data value.

18. (Original) The CAM device of Claim 17, wherein the priority circuit is configured to re-order the row indexes and match flags according to priority.

19. (Original) The CAM device of Claim 17, wherein the priority circuit further comprises:

means for storing the priority assigned to each array segment.

20. (Original) The CAM device of Claim 17, wherein the priority circuit further comprises:

a priority table having a plurality of rows each for storing the priority assigned to a corresponding array segment;

compare logic having a plurality of inputs to receive the priorities from the priority table and having an output;

a first multiplexer having a plurality of inputs to receive the priorities from the priority table, an output to generate a block priority, and a control terminal coupled to the output of the compare logic; and

a second multiplexer having a plurality of inputs each to receive the row index from a corresponding array segment, a control terminal coupled to the output of the compare logic, and an output to selectively output one of the row indexes.

21. (Currently Amended) The CAM device of Claim ~~19~~ 20, wherein each row of the priority table is responsive to a corresponding segment match flag.

22. (Original) The CAM device of Claim 17, wherein the priority circuit further comprises:

a plurality of first multiplexers, each having inputs to receive the segment match flags from the corresponding CAM block;

a plurality of re-order registers, each having an output coupled to a control terminal of a corresponding first multiplexer;

a priority encoder having a plurality of inputs, each coupled to an output of a corresponding first multiplexer;

a select circuit having a plurality of inputs to receive the row indexes and associated priorities from the corresponding CAM block, and having a plurality of control terminals each coupled to the output of a corresponding re-order register; and

a second multiplexer having a plurality of inputs coupled to corresponding outputs of the select circuit, a control terminal coupled to an output of the priority encoder, and outputs to generate the row index and priority of the matching data value that has the highest assigned priority.

23. (Original) The CAM device of Claim 17, wherein the priority circuit further comprises:

a plurality of first multiplexers, each having inputs to receive the segment match flags from the corresponding CAM block;

a plurality of re-order registers, each having an output coupled to a control terminal of a corresponding first multiplexer;

a priority encoder having a plurality of inputs, each coupled to an output of a corresponding first multiplexer;

a second multiplexer having a plurality of inputs coupled to the outputs of corresponding re-order registers, and a control terminal coupled to the output of the priority encoder; and

a third multiplexer having a plurality of input pairs, each for receiving the row indexes and priorities from the corresponding CAM block, and having a control terminal coupled to an output of the second multiplexer, and having outputs to generate the row index and priority of the matching data value that has the highest assigned priority.

24. (Original) A content addressable memory (CAM) device having a plurality of CAM blocks, each comprising:

an array of CAM cells divided into a plurality of segments, each array segment for storing a number of data values that are assigned the same priority;

means for generating a row index of a highest priority matching value;

means for storing address information for each array segment; and

means for comparing the row index with the address information to determine which priority the highest priority matching data value is assigned.

25. (Original) The CAM device of Claim 24, wherein each CAM block is assigned to store a unique range of data values.

26. (Original) The CAM device of Claim 24, further comprising:

means for extracting a selected portion of a search key; and

means for selectively enabling each CAM block in response to a comparison between the selected portion of the search key and the assigned range of data values for the corresponding CAM block.

27. (Original) The CAM device of Claim 24, wherein the address information comprises a start address for each array segment.

28. (Original) The CAM device of Claim 24, wherein the address information comprises an address range for each array segment.

29. (Original) The CAM device of Claim 24, wherein the means for generating and the means for comparing comprises a priority circuit.

30. (Original) The CAM device of Claim 29, wherein the priority circuit comprises an address table having a plurality of rows, each for storing address information for a corresponding array segment.

31. (Currently Amended) The CAM device of Claim ~~29~~ 30, wherein the means for comparing further comprises a compare circuit having first inputs to receive

the address information from the address table, a second input to receive the row index, and outputs to generate a priority select signal for each array segment.

32. (Original) The CAM device of Claim 31, wherein each CAM block further comprises:

a priority table having a plurality of rows, each for storing the priority assigned to a corresponding array segment and each responsive to a corresponding priority select signal.

33. (Original) The CAM device of Claim 32, wherein each CAM block further comprises:

means for storing the priorities assigned to each of the array segments.

34. (Original) The CAM device of Claim 24, wherein each CAM block further comprises:

means for re-ordering the priorities of the array segments.

35. (Original) The CAM device of Claim 34, wherein the means for re-ordering comprises a plurality of re-order registers, each for storing a re-order value.

36. (Original) A method of operating a content addressable memory (CAM) device having an array of CAM cells divided into a plurality of array segments, comprising:

assigning a different priority to each of the array segments;

storing address information for each array segment;

generating a row index of a highest priority matching data value stored in the array; and

comparing the row index with the address information to determine the priority of the highest priority matching data value.

37. (Original) The method of Claim 35, wherein the address information

comprises a start address for each array segment.

38. (Original) The method of Claim 35, wherein the address information comprises an address range for each array segment.

39. (Original) The method of Claim 35, further comprising:

storing the priorities assigned to the array segments in a priority table.

40. (Original) A method of operating a content addressable memory (CAM) device having an array of CAM cells divided into a plurality of array segments, comprising:

assigning a different priority to each of the array segments;

storing address information for each array segment;

generating a segment match flag and a row index of a matching data value stored in each array segment; and

comparing the row indexes with the address information to determine the priorities of the matching data values.

41. (Original) The method of Claim 40, further comprising:

re-ordering the row indexes and segment match flags according to their assigned priorities.